

# Victor A. Ying

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<b>RESEARCH INTERESTS</b>	Computer architecture, parallelizing compilers, parallel programming models, programmable accelerators, locality-aware execution, speculative execution, distributed systems, parallel algorithms, parallel runtimes
<b>EDUCATION</b>	<b>Massachusetts Institute of Technology</b> , Cambridge, Massachusetts Ph.D. in Electrical Engineering and Computer Science <i>anticipated 2022</i> S.M. in Electrical Engineering and Computer Science June 2019 <ul style="list-style-type: none"><li>Cumulative GPA: 4.93 / 5.00</li><li>Thesis title: Scaling Sequential Code with Hardware–Software Co-Design for Fine-Grain Speculative Parallelization</li><li>Thesis advisor: Daniel Sanchez</li></ul> <b>Princeton University</b> , Princeton, New Jersey B.S.E. <i>summa cum laude</i> in Electrical Engineering May 2016 <ul style="list-style-type: none"><li>Cumulative GPA: 3.95 / 4.00</li><li>Thesis title: Analyzing Decision Heuristic Effectiveness in Boolean Satisfiability Solvers</li><li>Thesis advisor: Sharad Malik</li></ul> <b>Selected coursework:</b> Computer architecture, operating systems, computer networks, algorithms, functional programming, program analysis, automated reasoning, logic design, image processing
<b>RESEARCH &amp; INDUSTRY EMPLOYMENT</b>	<b>Research Assistant and Edwin Webster Fellow</b> September 2016 – Present MIT Computer Science and Artificial Intelligence Lab, Cambridge, Massachusetts <ul style="list-style-type: none"><li>Supervisor: Daniel Sanchez</li><li>Design and evaluate enhancements to the Swarm architecture, a general-purpose multicore architecture for parallelizing challenging applications, through microarchitectural simulation.</li><li>Spearhead an LLVM/Clang-based compiler project to parallelize sequential C/C++ programs.</li></ul> <b>Research Intern</b> May – August 2018 NVIDIA Research, Westford, Massachusetts <ul style="list-style-type: none"><li>Develop analytical modeling tool for design space exploration and code optimization for efficient execution of linear algebra and machine learning workloads on a range of future hardware architectures.</li></ul> <b>Hardware Engineering Intern</b> May – August 2015 Pure Storage, Mountain View, California <ul style="list-style-type: none"><li>Modified firmware (C) and created tools (Python) for debugging prototype embedded system hardware through a serial connection. Developed a command line interface, a GDB server, and resource monitoring tools, using a binary packet protocol with checksums.</li></ul> <b>Software Engineering Intern</b> May – August 2014 Pure Storage, Mountain View, California <ul style="list-style-type: none"><li>Developed and deployed the first driver enabling integration of Pure Storage FlashArrays and OpenStack, an open-source cloud platform. Transferred ownership of this sales-driving feature to full-time engineers.</li><li>Wrote and open-sourced a Python library for managing FlashArrays, used for automated testing.</li></ul> <b>Technical Intern</b> June – August 2013 Northrop Grumman Electronic Systems, Baltimore, Maryland <ul style="list-style-type: none"><li>Optimized designs of RF electronics in radar systems using CAD and simulation tools.</li><li>Characterized prototypes to identify suspect connections and components to be redesigned.</li></ul> <b>Student Technician</b> June 2012 – June 2016 National Institute of Standards and Technology, Gaithersburg, Maryland <ul style="list-style-type: none"><li>Supervisor: Heather J. Patrick</li><li>Developed precise positioning software for robotic arms to enable repeatable reflectance measurements.</li><li>Modeled distortions in optical scattering measurements and automated post-processing correction factors.</li></ul>

<b>REFEREED CONFERENCE PAPERS</b>	<p>A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, <b>V. A. Ying</b>, A. Mukkara, R. Venkatesan, B. Khailany, S. W. Keckler, J. Emer “Timeloop: A Systematic Approach to DNN Accelerator Evaluation”, in <i>International Symposium on Performance Analysis of Systems and Software (ISPASS)</i>, 2019. Acceptance rate: 26/88 (30%)</p> <p>M. C. Jeffrey, <b>V. A. Ying</b>, S. Subramanian, H. R. Lee, J. Emer, and D. Sanchez, “Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism”, in <i>51st International Symposium on Microarchitecture (MICRO)</i>, 2018. Acceptance rate: 74/351 (21%)</p> <p>S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, <b>V. A. Ying</b>, J. Emer, and D. Sanchez, “Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism”, in <i>44th International Symposium on Computer Architecture (ISCA)</i>, 2017. Acceptance rate: 54/322 (17%)</p>																								
<b>OTHER PAPERS &amp; TALKS</b>	<p><b>V. A. Ying</b>, M. C. Jeffrey, and D. Sanchez, “Compiling Sequential Code for a Speculative Parallel Architecture”, selected from Student Research Competition to present full talk at <i>PLDI 2019</i></p> <p>S. Malik and <b>V. A. Ying</b>, “On the Efficiency of the VSIDS Decision Heuristic”, presented at <i>Theoretical Foundations of SAT Solving Workshop</i>, 2016.</p> <p>H. J. Patrick, C. J. Zarobila, T. A. Germer, <b>V. A. Ying</b>, C. A. Cooksey, and B. K. Tsai, “Tunable supercontinuum fiber laser source for BRDF measurements in the STARR II gonireflectometer”, in <i>Proceedings of SPIE Volume 8495</i>, 2012.</p>																								
<b>HONORS &amp; AWARDS</b>	<table border="0" style="width: 100%;"> <tbody> <tr> <td style="width: 80%;"><b>Best PhD Student Poster</b>, HPDC</td> <td style="text-align: right;">2019</td> </tr> <tr> <td><b>Second Place in Student Research Competition</b>, PLDI</td> <td style="text-align: right;">2019</td> </tr> <tr> <td><b>Best Poster</b>, Industry-Academia Partnership MIT Cloud Workshop</td> <td style="text-align: right;">2018</td> </tr> <tr> <td><b>Honorable Mention</b>, NSF Graduate Research Fellowship Program</td> <td style="text-align: right;">2018</td> </tr> <tr> <td><b>Edwin Webster Fellowship</b>, MIT Dept. of Electrical Engineering and Computer Science</td> <td style="text-align: right;">2016–2017</td> </tr> <tr> <td><b>Honorable Mention</b>, Ford Foundation Predoctoral Fellowship Program</td> <td style="text-align: right;">2016</td> </tr> <tr> <td><b>Highest Honors</b>, Princeton Dept. of Electrical Engineering</td> <td style="text-align: right;">2016</td> </tr> <tr> <td><b>Hisashi Kobayashi Prize</b>, Princeton Dept. of Electrical Engineering</td> <td style="text-align: right;">2016</td> </tr> <tr> <td><b>Sigma Xi</b>, Princeton Chapter</td> <td style="text-align: right;">2016</td> </tr> <tr> <td><b>Phi Beta Kappa</b>, New Jersey Beta Chapter</td> <td style="text-align: right;">2015</td> </tr> <tr> <td><b>Tau Beta Pi</b>, New Jersey Delta Chapter</td> <td style="text-align: right;">2014</td> </tr> <tr> <td><b>Shapiro Prize for Academic Excellence</b>, Princeton University</td> <td style="text-align: right;">2014</td> </tr> </tbody> </table>	<b>Best PhD Student Poster</b> , HPDC	2019	<b>Second Place in Student Research Competition</b> , PLDI	2019	<b>Best Poster</b> , Industry-Academia Partnership MIT Cloud Workshop	2018	<b>Honorable Mention</b> , NSF Graduate Research Fellowship Program	2018	<b>Edwin Webster Fellowship</b> , MIT Dept. of Electrical Engineering and Computer Science	2016–2017	<b>Honorable Mention</b> , Ford Foundation Predoctoral Fellowship Program	2016	<b>Highest Honors</b> , Princeton Dept. of Electrical Engineering	2016	<b>Hisashi Kobayashi Prize</b> , Princeton Dept. of Electrical Engineering	2016	<b>Sigma Xi</b> , Princeton Chapter	2016	<b>Phi Beta Kappa</b> , New Jersey Beta Chapter	2015	<b>Tau Beta Pi</b> , New Jersey Delta Chapter	2014	<b>Shapiro Prize for Academic Excellence</b> , Princeton University	2014
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<b>TEACHING &amp; MENTORSHIP</b>	<p><b>Chief Operating Officer</b> June 2012 – Present Kids Are Scientists Too, a national 501(c)(3) nonprofit</p> <ul style="list-style-type: none"> <li>• Expand after-school science programs for underprivileged elementary school students to nine states.</li> <li>• Mentor high school branch leaders and volunteers, who recruit peers, fundraise, and run science activities.</li> <li>• Manage finances, tax filings, nonprofit status, and KAST’s website and shared online resources for branches.</li> </ul> <p><b>Lab Assignment Writer and Teaching Assistant</b> Fall 2014, Fall 2015 ELE 206: Contemporary Logic Design, Princeton University</p> <ul style="list-style-type: none"> <li>• Held lab sessions and taught digital logic, RTL design, and FPGA synthesis to a class of 80 students.</li> <li>• Rewrote assignments to define and use a subset of Verilog and new cross-platform simulation software.</li> <li>• Overhauled the general-purpose processor project with a new ISA and software testing tools.</li> </ul> <p><b>Peer Academic Advisor</b> 2015–2016 Office of the Dean of Undergraduate Students, Princeton University</p> <ul style="list-style-type: none"> <li>• Engage first years in planning their academic paths, enrolling in courses, and adjusting to college academics.</li> </ul>																								

**Peer Tutor**

2013–2015

Office of the Dean of Undergraduate Students, Princeton University

- Tutor students in introductory mathematics, physics, and engineering classes.

*[Curriculum vitae compiled on 2019-09-04]*